CLAIMS

Please cancel claims 5, 8, 14, 20, 29, 31, 37, 49, 52, and 54-55 without prejudice or disclaimer. Please amend claims and add new claims as shown in the following claim listing.

1. (Currently amended) A method comprising:

checking a current clock period when a memory is accessed, the current clock period being one of a given number of clock periods; and

setting a usage bit corresponding to the current clock period during a writeback cycle to write data read from the memory back to the memory, the usage bit indicating usage information for the data,

wherein the memory is non-volatile destructive read cache memory.

2. (Previously presented) The method of claim 1, comprising:

erasing usage bits corresponding to a new clock period.

3. (Previously presented) The method of claim 2, wherein erasing includes erasing usage bits at once.

4. (Previously presented) The method of claim 1, comprising:

resetting usage bits in response to changing an address or tag for the memory; and

setting a usage bit corresponding to a current clock period.

5. (Canceled).

6. (Previously presented) The method of claim 1, wherein the given number of clock periods is four.

7-8. (Canceled).

9. (Currently amended) The method of ~~claim 8~~claim 1, wherein the ~~destructive read~~ memory is one of a polymer ferroelectric RAM, a magnetic RAM or a core memory.

10. (Canceled).

11. (Previously presented) The method of claim 1, comprising:

de-allocating data in the memory based upon usage bits.

12. (Currently amended) A memory comprising:

an area to store data; and

an area to store metadata for the data, the metadata including a plurality of usage bits to indicate usage information for entries in the memory, a usage bit to indicate whether a corresponding entry was accessed during a corresponding one of a given number of clock periods,

wherein the memory is ~~a~~ non-volatile destructive read cache memory and wherein a usage bit for an entry read from the memory is to be updated during a writeback cycle to write the read entry back to the memory.

13. (Original) The memory of claim 12, wherein the usage information is a least recently used information.

14. (Canceled).

15. (Previously presented) The memory of claim 12, wherein the given number of clock periods is four.

16. (Canceled).

17. (Currently amended) The memory of claim 12, wherein the ~~destructive read~~ memory ~~is one of a~~comprises polymer ferroelectric ~~RAM, a magnetic RAM or a core~~ memory.

18. (Currently amended) A system comprising:

a magnetic memory device;

~~a~~ non-volatile destructive read memory to cache data for the magnetic memory device and to store metadata for the data, the metadata including a plurality of usage bits to indicate usage information for entries in the memory, a usage bit to indicate whether a corresponding entry was accessed during a corresponding one of a given number of clock periods; and

a memory controller to update a usage bit for an entry read from the memory during a writeback cycle to write the read entry back to the memory, the memory controller to de-allocate an entry using usage bits.

19. (Original) The system of claim 18, wherein the usage information is a least recently used information.

20. (Canceled).

21. (Previously presented) The system of claim 18, wherein the given number of clock periods is four.

22. (Canceled).

23. (Currently amended) A method comprising:

storing usage bits to indicate usage information for entries in a memory, a usage bit to indicate whether a corresponding entry was accessed during a corresponding one of a predetermined number of clock periods; and

updating a usage bit for an entry read from the memory during a writeback cycle to write the read entry back to the memory.

wherein the memory is non-volatile destructive read cache memory.

24. (Original) The method of claim 23, wherein the usage information is a least recently used information.

25. (Canceled).

26. (Previously presented) The method of claim 23, wherein updating a usage bit comprises:

checking a current clock period when the memory is accessed, the current clock period being one of a predetermined number of clock periods; and

setting a usage bit corresponding to the current clock period.

27. (Previously presented) The method of claim 26, comprising:

erasing usage bits corresponding to a new clock period.

28. (Previously presented) The method of claim 26, comprising:

resetting usage bits when an address or tag for an entry is changed; and

setting a usage bit corresponding to a current clock period.

29. (Canceled).

30. (Previously presented) The method of claim 26, wherein the predetermined number of clock periods is four.

31. (Canceled).

32. (Currently amended) A machine readable medium having executable instructions comprising:

a first group of executable instructions to check a current clock period when a memory is accessed, the current clock period being one of a predetermined number of clock periods; and

a second group of executable instructions to set a usage bit corresponding to the current clock period during a writeback cycle to write data read from the memory back to the memory, the usage bit indicating usage information for the data,

wherein the memory is non-volatile destructive read cache memory.

33. (Previously presented) The medium of claim 32, comprising:

a third group of executable instructions to erase usage bits corresponding to a new clock period.

34. (Previously presented) The medium of claim 32, comprising:

a third group of executable instructions to reset usage bits in response to changing an address or tag for the memory, and to set a usage bit corresponding to a current clock period.

35. (Currently amended) A machine readable medium having executable instructions comprising:

a first group of executable instructions to store usage bits to indicate usage information for entries in a memory, a usage bit to indicate whether a corresponding entry was accessed during a corresponding one of a predetermined number of clock periods; and

a second group of executable instructions to update a usage bit for an entry read from the memory during a writeback cycle to write the read entry back to the memory,

wherein the memory is non-volatile destructive read cache memory.

36-41. (Canceled).

42. (Previously presented) An apparatus comprising:

a non-volatile destructive read memory to cache data for a storage device and to store usage bits to indicate usage information for the cache data stored in the non-volatile destructive

read memory, a usage bit to indicate whether a corresponding entry was accessed during a corresponding one of a predetermined number of clock periods,

wherein a usage bit is updated during a writeback cycle to rewrite a corresponding entry destroyed during a read from the non-volatile destructive read memory back to the non-volatile destructive read memory.

43. (Currently amended) The apparatus of claim 42, wherein the non-volatile destructive read memory ~~is a polymer ferroelectric random access memory (PFRAM), a magnetic RAM (MRAM), or a core memory~~comprises magnetic random access memory (MRAM).

44. (Previously presented) The apparatus of claim 42, wherein the storage device is a magnetic or optical memory device.

45. (Previously presented) The apparatus of claim 42, comprising:
a cache controller coupled to the non-volatile destructive read memory; and
a main memory coupled to the cache controller.

46. (Currently amended) The apparatus of claim 42, wherein the non-volatile destructive read memory ~~is a~~comprises polymer ferroelectric memory.

47. (Canceled).

48. (Previously presented) The apparatus of claim 42, wherein the usage information is least recently used information.

49-50. (Canceled).

51. (Currently amended) An apparatus comprising:

memory to store data and usage bits to indicate usage information for entries in the memory, a usage bit to indicate whether a corresponding entry was accessed during a corresponding one of a predetermined number of clock periods,

wherein a usage bit for an entry read from the memory is to be updated during a writeback cycle to write the read entry back to the memory,

wherein the memory comprises non-volatile destructive read cache memory.

52. (Canceled).

53. (Previously presented) The apparatus of claim 51, wherein usage information comprises least recently used information.

54-56. (Canceled).

57. (New) The memory of claim 12, wherein the memory comprises magnetic random access memory (MRAM).

58. (New) The memory of claim 12, wherein the memory comprises core memory.

59. (New) The system of claim 18, wherein the memory comprises polymer ferroelectric memory, magnetic random access memory (MRAM), or core memory.

60. (New) The method of claim 23, wherein the memory comprises polymer ferroelectric memory, magnetic random access memory (MRAM), or core memory.

61. (New) The medium of claim 32, wherein the memory comprises polymer ferroelectric memory, magnetic random access memory (MRAM), or core memory.

62. (New) The medium of claim 35, wherein the memory comprises polymer ferroelectric memory, magnetic random access memory (MRAM), or core memory.

63. (New) The apparatus of claim 42, wherein the non-volatile destructive read memory comprises core memory.

64. (New) The apparatus of claim 51, wherein the memory comprises polymer memory.

65. (New) The apparatus of claim 51, wherein the memory comprises ferroelectric memory.

66. (New) The apparatus of claim 51, wherein the memory comprises magnetic random access memory (MRAM).

67. (New) The apparatus of claim 51, wherein the memory comprises core memory.